Scalable Parasitic Charge Redistribution: Design of High-Efficiency Fully Integrated Switched-Capacitor DC-DC Converters

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***Abstract*—This paper introduces a technique, called Scalable Parasitic Charge Redistribution (SPCR), that reduces the parasitic Bottom-Plate (BP) losses in fully-integrated Switched-Capacitor (SC) voltage regulators up to any desired level. This is realized by continuously redistributing parasitic charge in-between phase-shifted converter cores. Because earlier models described the ratio of this parasitic coupling to the flying capacitance as the only limiting factor on the achievable fully-integrated efficiency, the use of SPCR allows SC converters to achieve efficiencies previously deemed impossible. Transistor leakage is shown to be another limiting factor and is added to existing models which are then used to prove the effectiveness of SPCR over a wide range of power densities (up to $10W/mm^2$) and technological parameters. The implementation of SPCR requires little overhead thanks to the use of Charge Redistribution Buses. A 1/2 converter is fabricated in a 40nm bulk CMOS technology that demonstrates SPCR by achieving a record efficiency for fully-integrated closed-loop SC converters of 94.6%.**

***Index Terms*—Switched-Capacitor, DC-DC, Power management, Fully Integrated, Scalable Parasitic Charge Redistribution, High Efficiency, Loss Model, Optimization, Parasitic, Bottom-Plate Losses**

I. Introduction

In the past few years the delivery of power to Integrated Circuits (IC) has become increasingly difficult for a wide range of applications. At the core of this issue lies the continued scaling of supply voltages. Lowering the supply voltage of applications has simultaneously lead to an increase of their intake current, which has in turn increased the resistive IR losses and di/dt effects in the Power Delivery Network (PDN). In high-end CPU processors, for example, a larger and larger proportion of the I/O pins is needed for power and ground [1] [2], while in recent smartphone processors, more than 30% of the energy is lost due to PDN- and Power Management IC (PMIC)-induced voltage margins [3].

As a solution to this problem, many have suggested moving part of the voltage conversion on chip using Fully Integrated Voltage Regulators (FIVR) [3] [4] [5]. Doing so would reduce the intake current by the achieved on chip Voltage Conversion Ratio (VCR) and allow for closer regulation. PDN and regulator induced voltage margins can thus be significantly reduced, and the overall system efficiency is increased. Furthermore, combined with techniques such as Dynamic Voltage and Frequency Scaling (DVFS), having per-core or per-domain voltage conversion and regulation could enable further energy savings [6]. However, to warrant the use of FIVR's, it is crucial that the aforementioned gains do not get eclipsed by the decreased FIVR efficiency compared to external PMIC's, caused by the lower quality of passives and larger parasitics in the monolithic context. Consequently, the FIVR's efficiency is often considered to be its most important specification [3]. Another important attribute of a FIVR is its output power density which determines its economic feasibility for a given application. For certain applications, achieving sufficient power density in a fully-integrated environment is still the subject of ongoing research.

Switched-Capacitor (SC) converters have become the most popular type of FIVR because, contrary to inductive converters, they only use switches and capacitors, both of which are native to CMOS, and scale well into deep sub-micron nodes. In the optimization space of this type of converter there is a clear trade-off between power and efficiency, which is especially pronounced at high output power densities. Here, the generally limited capacitance density available on-chip, together with switch conductance- and drive losses, restrict the converter's efficiency [7]. For decreasing output power, however, less and less efficiency can be gained until eventually a maximum is hit. According to previous models [7], this maximum obtainable efficiency of a SC DC-DC converter is described by

$$\eta_{max} = \frac{1}{1 + \sqrt{\alpha_{BP} K_{BP} K_c}}, \tag{1}$$

and depends on three factors. K_{BP} and K_c are topological constants whose optimal value is determined by

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the converter's VCR, while the other, α_{BP}, is the relative size of the parasitic coupling of the flying capacitor, the so-called Bottom-Plate (BP) capacitance, to the size of the flying capacitance itself. This leads to the interesting observation that the efficiency ceiling is seemingly only dependent on the capacitor quality. Later in this paper, it will be shown that also the quality of transistors is important.

Generally speaking, the larger the relative distance between the converters in- and output voltage, and the larger α_{BP}, the lower the efficiency that can be obtained. With α_{BP} typically around 1.5% for Metal-Oxide-Metal (MOM) and Metal-Insulator-Metal (MIM), and 7% for Metal-Oxide-Semiconductor (MOS) capacitors, an SC 1/2 converter could theoretically achieve efficiencies up to 89% and 79% respectively. Due to additional losses (control, leakage, interconnect, ...) the effective efficiency ceiling is lower, but its existence is still confirmed by previous work [8] [9]. The highest reported fully integrated closed-loop converter efficiencies in baseline CMOS are 87% [10], although at a more favorable VCR of 2/3, and 85% [11], both using MIM capacitors. Higher efficiencies have been demonstrated using either open-loop converters with VCR's very close to 1:1 (95% in 15/16) [12], or high-density Deep-Trench (88% in 1/2) [13] or Ferro-Electric (91% in 1/2) [14] capacitors, which have reportedly up to 25 times lower α_{BP}. However, these capacitors are not part of baseline CMOS and thus require additional masks and costs.

Due to its importance on the achievable efficiency, some have suggested to short the BP nodes of two converters in anti phase during the dead time in-between phase transitions, effectively redistributing half of the parasitic charge from the discharging BP capacitor to the charging one [1] [15]. The supply voltage consequently only needs to supply the remaining half to charge the BP capacitor, resulting in a 2x reduction in BP losses. While effective, this method does not scale to higher levels of redistribution because it still uses the same two-phase control signals for the converter.

This paper is organized as follows. In Section II, a technique that reduces the BP losses up to any desired level, called Scalable Parasitic Charge Redistribution (SPCR), is introduced. Its effect on the design space of fully-integrated SC converters will be explored in Section III. Section IV goes into more detail how SPCR can be efficiently implemented using an example implementation. Measurement results, showing the effectiveness of SPCR in a realized converter, are discussed in Section V. Finally, Section VI highlights the important conclusions of this work in a brief summary.

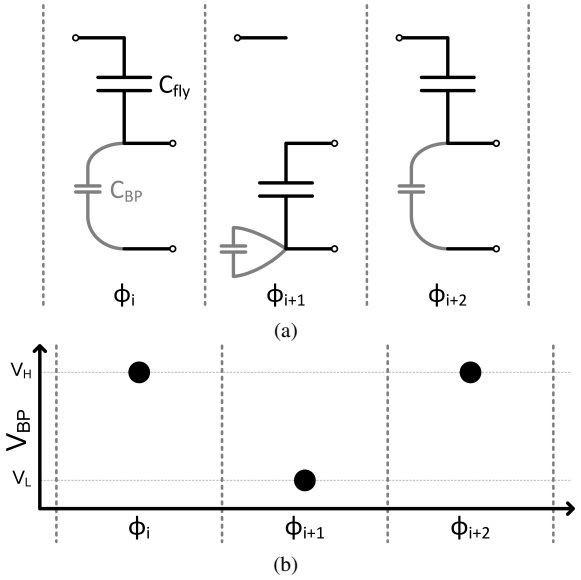

Fig. 1. Regular switched capacitor converter. (a) Normal representation using lumped capacitors. C_{fly} and C_{BP} are the flying and parasitic capacitor respectively. (b) Alternative representation used in this paper.

II. Scalable Parasitic Charge Redistribution

A. Regular Switched-Capacitor Converters

In Fig. 1a the general working principle of a regular SC converter's flying capacitor is portrayed. Each phase, a certain amount of charge is pumped by the flying capacitor, depending on the voltage mismatch between both domains and the size of the capacitor, C_{fly}. However, in order to keep this process running, once every other phase, charge needs to be invested into the parasitic BP capacitor. This parasitic charge, q_{par}, scales with the size of the parasitic coupling, C_{BP}, and the voltage step between both domains, ΔV. The former is largely determined by the process technology and the type of capacitors used. Instead, ΔV will be key in reducing the associated BP losses up to any desired level. Figure 1b shows an alternative representation of the same converter but with additional emphasis on the bottom-plate voltage, V_{BP}. This representation will be used throughout this paper.

A popular technique used in SC converters in literature is Time-Interleaving (TI) or Multi-phasing [16] [17]. Here, the converter is split up into N smaller converter cores. An example TI converter is shown in Fig. 2. Each clock edge, the 2 cores that have been in the high/low state the longest, transition to the next state by fully charging/discharging their V_{BP} to V_H/V_L. Consequently, while this technique does reduce the output voltage ripple significantly [16], the BP losses remain unchanged.

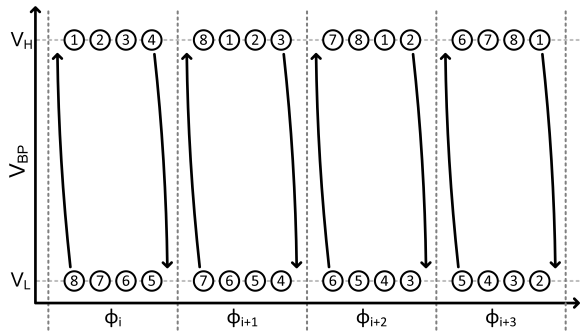

Fig. 2. An example Time-Interleaved switched-capacitor converter with 8 cores. Each labeled circle represents a different converter core. Arrows represent actions during phase transition.

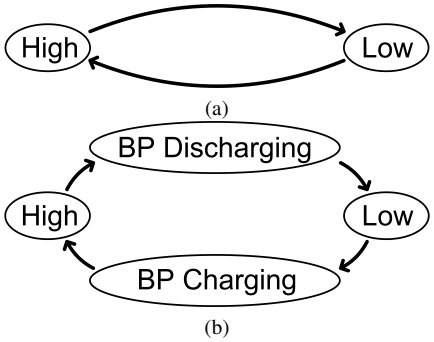

Fig. 3. State transitions of (a) a regular SC converter or a time interleaved converter core and (b) a SPCR converter core

B. Charge Redistribution

The general idea of SPCR is straightforward: Instead of having N TI converter cores working in parallel to one another, the cores will actively and continuously redistribute their parasitic charge amongst each other to reduce the BP losses and thus enhance their efficiency. To this end, a dedicated BP charging and a dedicated BP discharging state are introduced (Fig. 3). Rather than transitioning from a high state directly to a low state, a core will first enter the dedicated BP discharging state. Likewise, a core will go through the BP charging state when going from the low to the high state.

In Fig. 4 an example SC converter using SPCR is shown. Cores that are neither in the regular high, nor in the regular low state, are instead in the BP charging or discharging state. Here, all the regular power transistors are non-conducting and the core itself can only be at a set number of intermediate levels, chosen during design time. At every clock edge, each BP charging core is paired up with the BP discharging core which is in the closest, yet higher intermediate level. By shorting the BP nodes of each pair, their V_{BP}'s average out by transferring charge from the BP discharging to the BP charging core. This is called a Charge Redistribution Step (CRS) and results in all paired BP charging cores going up,

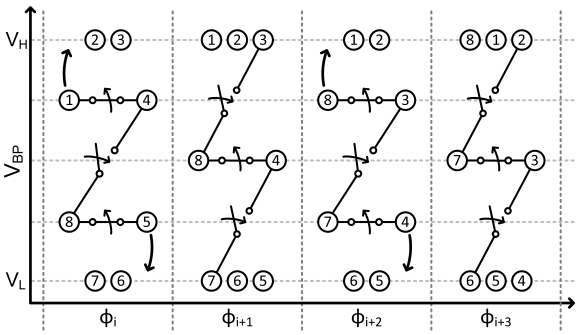

Fig. 4. An example switched-capacitor converter using Scalable Parasitic Charge Redistribution (SPCR) with 8 cores and 3 Charge Redistribution Steps (CRS). Arrows represent actions during phase transitions.

and all paired BP discharging cores going down one intermediate level. BP charging/discharging cores which are already at the highest/lowest intermediate level, and can consequently pair up no more, are instead pulled up/down to the high/low state. Furthermore, to keep this process going, every two phases, the two cores that have been in the high/low state for the longest time, are transferred to the BP discharging/charging state. The end result is that the low to high transition is now completed approximately adiabatically using a fixed number of CRS, equal to the number of intermediate levels and that V_H only needs to supply enough charge to pull the core up to the high state, which is in general $(CRS+1)$ times lower than the charge without SPCR. The BP losses are consequently also reduced by the same factor:

$$P_{BP,SPCR} = \frac{P_{BP,regular}}{CRS+1}. \tag{2}$$

Because all cores are phase-shifted versions of each other, the necessary connections between cores and timing of the charge exchanges are known at design time, significantly simplifying the design of this kind of SC converter. The phases as shown in Fig. 4 are also stable and require no initialization. This can intuitively be explained as follows: Because every CRS is an averaging operation, the voltage of an intermediate level will be the average of its surrounding levels. The intermediate levels will subsequently naturally spread evenly between the boundary conditions of V_H and V_L.

SPCR can be implemented no matter the switched-capacitor topology, and thus VCR, by applying the technique to each unique capacitor separately. For a SC converter using SPCR there are two important design parameters: The total number of cores, N, and the number of intermediate levels or charging steps, CRS. The only condition for SPCR to work in theory is given by equation (3). If it is not met, there are simply not enough cores to pair up each phase transition.

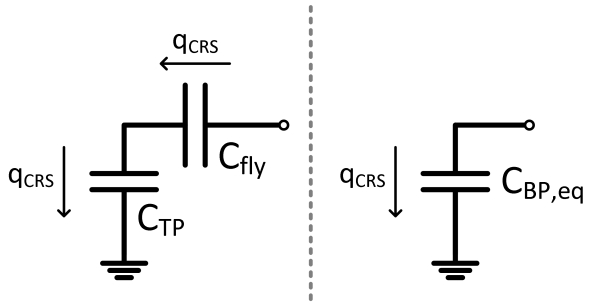

Fig. 5. Charge transfers during single Charge Redistribution Step (CRS) of a flying capacitor with parasitic Top-Plate (TP) coupling and the equivalent Bottom-Plate (BP) coupling.

$$N \geq CRS + 1 \tag{3}$$

C. Top Plate

While in literature the losses corresponding to the parasitic coupling of the flying capacitor or often referred to as Bottom-Plate losses, the equivalent parasitic capacitor is not necessarily entirely or even partly connected to the flying capacitor bottom-plate node. Metal-finger based MOM capacitors, for example, generally have equal coupling on the Top Plate (TP) and the BP. At the same time, capacitors with an asymmetrical parasitic coupling can still be connected such that the node with the highest voltage has most of the coupling. Using SPCR with capacitors which have significant TP coupling raises the interesting question: Should the charge redistribution (also) take place at the top side of the flying capacitor?

In Fig. 5 a single CRS of a core in the BP charging state which has a certain TP coupling C_{TP} is shown. This situation can be modeled with an equivalent $C_{BP,eq}$, shown in the same figure, which is the series of its parts.

If C_{TP} is sufficiently small compared to C_{fly}, $C_{BP,eq}$ will be approximately equal to C_{TP} and the voltage step on the top plate can be approximated by the voltage step on the BP plate. The parasitic charge on the TP can thus indeed be redistributed through the BP node. However, two important second-order effects occur when doing so. First, for step-down converters, the total TP swing is generally larger than the total BP swing due to the fact that such a converter transfers charge from a high- to a low voltage by charging its flying capacitors in a high- and discharging the same capacitors in a low voltage domain. Consequently, this pumped charge, ultimately meant for the converter output, is added as an extra voltage difference to the TP swing, as shown in Fig. 6a. This extra swing will not be redistributed through this method which means that more charge will need to be supplied in the transition to the high state. The parasitic coupling losses will thus be higher than described by

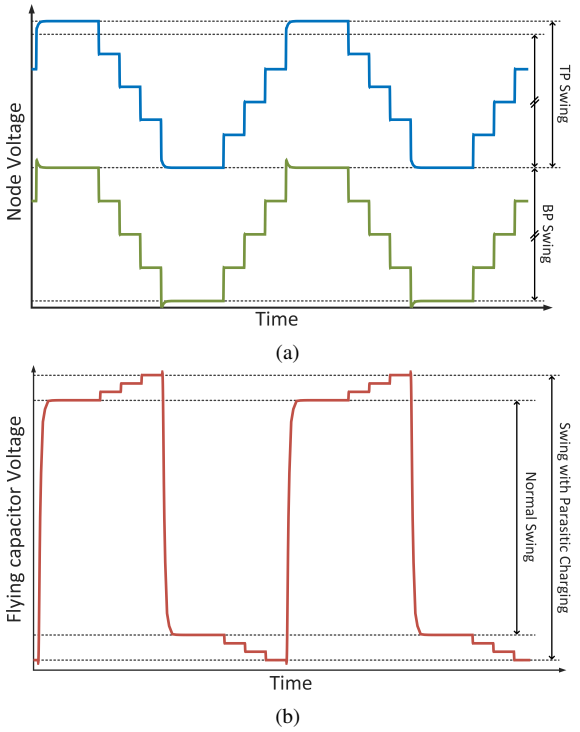

Fig. 6. Simulated waveforms of (a) the Top-Plate (TP) and Bottom-Plate node voltages and (b) the flying capacitor voltage, of a SPCR SC converter redistributing TP charge through the BP node.

equation 2. At the same time, though, a CRS of the TP coupling through the BP node also charges C_{fly} (Fig. 6b). The authors refer to this effect as *parasitic charging*. In the case of a step-down converter this additional charge is generally in the same direction as the regular pumped charge (occurring in the high and low state) and thus more charge is pumped to the converter output than usual. In terms of losses, both effects were found to cancel each other out. In fact, in a direct comparison of a converter with only TP coupling to one with only BP coupling, no significant change in efficiency was witnessed. The TP coupling converter does, however, always produce a higher output voltage.

Redistributing charge from the TP and BP nodes simultaneously has the undesirable effect of also re-distributing charge on C_{fly} meant for the output of the converter. This significantly increases the converter's output resistance and should therefore not be considered.

III. Switched-Capacitor Model and Optimization with SPCR

A. Regular SC Losses

An SC converter can be modeled as an ideal voltage converter, followed by a finite output resistance and an extra parasitic shunt resistor [7] [15]. The finite output resistance is caused by a combination of capacitor

TABLE I
OVERVIEW OF SWITCHED-CAPACITOR TOPOLOGICAL FACTORS.

Topological factor	Formula
K_c	$\sum_{caps,i} \frac{a_{c,i}^2}{C_{\%,i}}$
K_s	$\sum_{switches,i} \frac{a_{r,i}^2}{G_{\%,i}}$
K_{BP}	$\sum_{caps,i} C_{\%,i}\left(\frac{\Delta V_i}{V_{out}}\right)^2$

charge sharing- or Slow-Switching Limit (SSL) losses and switch resistance- or Fast-Switching-Limit (FSL) losses, respectively given by

$$P_{SSL} = \frac{I_L^2}{f_{sw} C_{fly}} K_c, \tag{4}$$

$$P_{FSL} = \frac{I_L^2}{G_{tot}} \frac{K_s}{D}, \tag{5}$$

with I_L the load current, f_{sw} the switch frequency, C_{fly} the total flying capacitance, K_c a topological factor dependent on the capacitor charge multipliers $\boldsymbol{a_{c,i}}$ and relative capacitor sizes $\boldsymbol{C_{\%,i}}$ [18], G_{tot} the total switch conductance, D the switch duty cycle and K_s a topological factor dependent on the switch charge multipliers $\boldsymbol{a_{r,i}}$ and relative switch sizes $\boldsymbol{G_{\%,i}}$ [18]. The parasitic losses, on the other hand, are in current models primarily attributed to the dynamic BP and transistor losses, described by

$$P_{BP} = \alpha_{BP} C_{fly} f_{sw} V_{out}^2 K_{BP}, \tag{6}$$

$$P_{trans} = \alpha_t G_{tot} f_{sw} V_{trans}^2, \tag{7}$$

respectively, with V_{out} the output voltage, K_{BP} the topological capacitor node swing factor [19], α_t the transistor capacitance per unit conductance and V_{trans} the transistor voltage swing. Note that (7) assumes only one type of transistor is used and that V_{trans} is equal for all transistors. An overview of all topological factors is given in Table I.

B. Transistor Leakage

According to (1), using SPCR could lead to converter efficiencies arbitrarily close to 100%. This apparent lack of trade-off hints to the need to include more loss contributors in the SC model. Therefore, the effect of transistor leakage is investigated.

A (NMOS) transistor in the non-conducting state has a drain to source current, I_{subt}, and a reverse gate tunneling current from drain to the gate, I_{rev}. In the conductive state there also is a gate tunneling current, I_{gate}, from the gate to the channel [20]. The associated losses are given by

$$P_{l,nc} = \sum_{switches,i} (1 - D_i) V_{block,i} \big(I_{subt,i} + I_{rev,i}\big) \tag{8}$$

$$P_{l,c} = \sum_{switches,i} D_i V_{trans,i} I_{gate,i}. \tag{9}$$

with D_i the switch duty cycle and $V_{block,i}$ the blocking voltage. Assuming that V_{block}, V_{trans} and D are identical for all switches, the total leakage losses can be simplified to

$$P_l = \alpha_l(D) G_{tot} V_{out}^2, \tag{10}$$

where α_l is the normalized average leak-to-conductance conductance ratio,

$$\alpha_l(D) = (1 - D)\alpha_{l,nc} \frac{V_{block}^2}{V_{out}^2} + D\alpha_{l,c} \frac{V_{trans}^2}{V_{out}^2}, \tag{11}$$

and $\alpha_{l,c}$ and $\alpha_{l,nc}$ are the conductance ratio's of the conducting- and non-conducting phase respectively. Similarly to the dynamic losses, these leakage losses are modeled as an extra shunt resistor.

C. Regular SC optimization

Combining all these losses together, one can describe the total loss of a SC converter as

$$P_{loss} = P_{SSL} + P_{FSL} + P_{BP} + P_{trans} + P_l. \tag{12}$$

Note that while the total conduction losses (combination of P_{SSL} and P_{FSL}) can be more accurately formulated using either a quadratic sum [15] or variations thereof [21], the addition used here allows us to simplify the equations and still come up with insightful conclusions, similar to the approach in [7]. Also, rather than optimizing P_{loss}, the normalized losses $P_N = \frac{P_{loss}}{P_L}$, with P_L the load power, are used. The latter has the advantage of being directly related to the converter's efficiency, without needing another parameter as $\eta = \frac{1}{1+P_N}$

For the regular SC converter, the converter frequency, f_{sw}, and total transistor conductance, G_{tot}, are considered to be the most important design parameters. A third parameter, which is usually set by the converter's specifications is the output power density, P_D. Optimizing the normalized losses for these parameters, under the assumption that the total transistor area is negligible compared to the capacitor area, gives the following conditions:

$$\frac{\partial P_N}{\partial f_{sw}} = 0 \Leftrightarrow P_{SSL} = P_{BP} + P_{trans}, \tag{13}$$

$$\frac{\partial P_N}{\partial G_{tot}} = 0 \Leftrightarrow P_{FSL} = P_l + P_{trans}, \tag{14}$$

$$\frac{\partial P_N}{\partial P_D} = 0 \Leftrightarrow P_{FSL} + P_{SSL} = P_{BP} + P_{trans} + P_l. \tag{15}$$

Thus, regardless of power density, (13) and (14) must be satisfied in an optimal design, which implies the total conductance losses should always be at least as large as the sum of the others combined. The maximum efficiency, on the other hand, is achieved when also (15) is met. In this case, the output power density will tend to zero, the dynamic transistor charging losses, P_{trans}, will be zero, and f_{sw} and G_{tot} will be such that $P_{SSL} = P_{BP}$ and $P_{FSL} = P_l$, respectively. The corresponding minimal normalized losses are

$$P_{N,min} = \frac{2\sqrt{P_{SSL}P_{BP}} + 2\sqrt{P_{FSL}P_l}}{P_L} \tag{16}$$

$$P_{N,min} = 2\sqrt{\alpha_{BP}K_{BP}K_c} + 2\sqrt{\alpha_l(D)\frac{K_s}{D}}. \tag{17}$$

Thus, similarly to the capacitors, the quality of the transistors, determined by the conductance ratio, puts a limit on the maximum obtainable efficiency of a switched-capacitor converter.

D. SPCR optimization

Using Scalable Parasitic Charge Redistribution will change the losses of an SC converter in three ways.

1) BP losses: The BP losses will be reduced according to (2), assuming no second-order effects, discussed in section II-C, take place.

2) Duty cycle: Due to the dedicated BP charging/discharging state, the duty cycle of the regular power transistors in a two-phase converter are lowered to

$$D = \frac{N - CRS}{2N}, \tag{18}$$

which will increase P_{FSL} and change α_l.

3) Charge Redistribution Transistors (CRT): Because each transistor is shared between two cores, only $\frac{CRS}{2}$ CRT's per core are needed to perform the parasitic charge exchanges. $\frac{N \cdot CRS}{2}$ extra transistors are consequently required in total, which will all add dynamic transistor- and leakage losses. Assuming each CRT is sized such that 3 RC time constants equal one CRS time period, the total CRT conductance, G_{CRT}, and associated losses, using (7) and (10), can be respectively described by

TABLE II
SUMMARY OF LOSS CONTRIBUTORS INFLUENCED BY SPCR DESIGN PARAMETERS.

Loss contributor	**Scaling**
Parasitic Bottom-Plate	$\frac{1}{CRS+1}$
Power Transistor FSL	$\frac{2N}{N-CRS}$
Power Transistor Leakage	$\alpha_l\left(\frac{N-CRS}{2N}\right)$
CRT Overhead Gate	$N \cdot CRS$
CRT Overhead Leakage	$\alpha_l\left(\frac{1}{N}\right) \cdot N \cdot CRS$

$$G_{CRT} = 3\alpha_{BP} f_{sw} C_{fly} \frac{N \cdot CRS}{2}, \tag{19}$$

$$P_{trans,CRT} = 3\alpha_{BP}\alpha_t f_{sw}^2 C_{fly} V_{trans}^2 \frac{N \cdot CRS}{2}, \tag{20}$$

$$P_{l,CRT} = 3\alpha_{BP}\alpha_l (N^{-1}) f_{sw} C_{fly} V_{out}^2 \frac{N \cdot CRS}{2}. \tag{21}$$

The scaling of each loss contributor that is influenced by either N or CRS is summarized in Table II. No straight-forward model is found to determine the optimal N or CRS, which means that in a practical design a numerical optimizer is required. For the optimal normalized losses on the other hand, the following approximation, derived using asymptotic analysis, is proposed:

$$P_{N,SPCR,min} \approx \frac{3\sqrt{\alpha_{BP}K_{BP}K_c}}{\sqrt[6]{\frac{K_{BP}}{\alpha_l(0)}}} + 2\sqrt{\frac{\alpha_l(2^{-1})}{2^{-1}}K_s}. \tag{22}$$

Note the similarities between (17) and (22). Because the duty cycle of a two-phase converter is 0.5, the second term is the same in both instances, while the first is $\frac{2}{3}\sqrt[6]{\frac{K_{BP}}{\alpha_l(0)}}$ times smaller in the SPCR case. Figure. 7 provides a visual comparison. As expected, for very large conduction ratios, the second term in (22) dominates, and the losses are very similar. For smaller ratios, however, SPCR significantly reduces the impact of the BP coupling, and allows for much higher efficiencies to be achieved. In general, the higher the transistor quality, the higher the gain with SPCR.

In Fig. 8, a comparison is made for practical power densities. SPCR increases the efficiency over the entire power density range of $10\mu W/mm^2$ to $10W/mm^2$ and for all parameter variations. At high power densities, the improvement due to SPCR is invariant to the conductance ratio, which means low-V_T or High-Performance

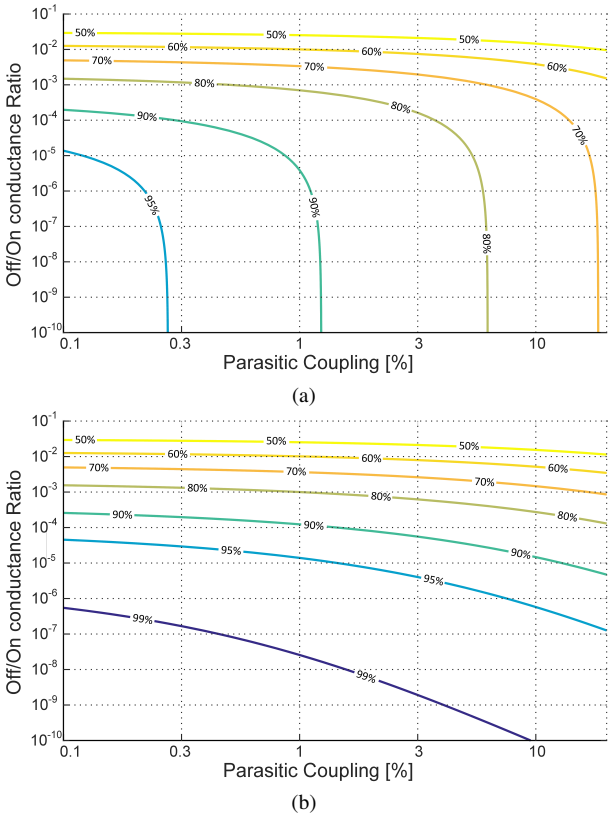

Fig. 7. Maximum achievable efficiency of (a) a regular 2:1 SC converter and (b) a 2:1 converter using SPCR.

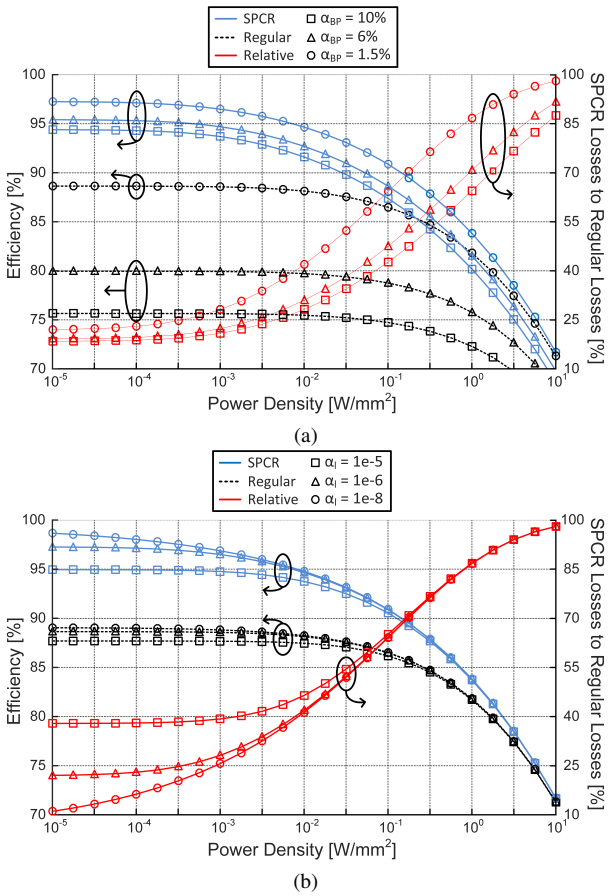

Fig. 8. Comparison of the efficiency and normalized losses of a regular 2:1 SC converter to one with SPCR for (a) a fixed α_l of 1e-6 and (b) a fixed α_{BP} of 1.5%.

(HP) devices can be used. Furthermore, the impact of α_{BP} is noticeably reduced. For lower power densities, on the other hand, the use of Low-Power (LP) or high-V_T devices provides a significant efficiency boost.

IV. SPCR Implementation

To verify the obtainable efficiencies of the SPCR technique, a fully-integrated 2:1 SC converter was designed using 16 cores and 9 CRS, thus reducing the BP losses tenfold. A system overview of the converter is shown in Fig. 9. Note that because SPCR naturally extends on the time-interleaving concept, no decoupling is used at the output of the converter.

A. Charge Redistribution Bus

For the charge exchanges to take place, a total of 72 different core interconnections are needed, which will all add overhead area and extra losses due to charging and discharging of their parasitic coupling. Instead, 8 Charge Redistribution Buses (CRB) are used, as shown in Fig. 10. The principle of a CRB is very similar to a data bus: When two BP nodes need to be shorted, they are both connected to the same bus. Furthermore the bus they use depends on their resulting intermediate voltage level after their V_{BP}'s average out. The end result is that significantly less area overhead is needed and that the voltage swing, and associated parasitic loss, on each CRB is approximately zero, effectively making them DC voltage rails. Normally this would require 9 buses (one for each intermediate level). In this design, however, the 0.5xV_{out} bus is replaced with a short connection between each in- and anti-phase pair which are already placed physically close to each other because they share most control signals. Also, note that while with this topology only one set of CRB's is necessary, if a topology has more than one capacitor with a unique BP swing, each will require its own set of CRB's.

B. Control

The output of the converter is regulated at a fixed voltage V_{ref} using a lower-bound hysteretic controller clocked at 50MHz [22]. Because for an uneven CRS a core is only switched to V_{out} once every other phase, each comparator trigger event needs to cause two phase transitions to assure a fast response time.

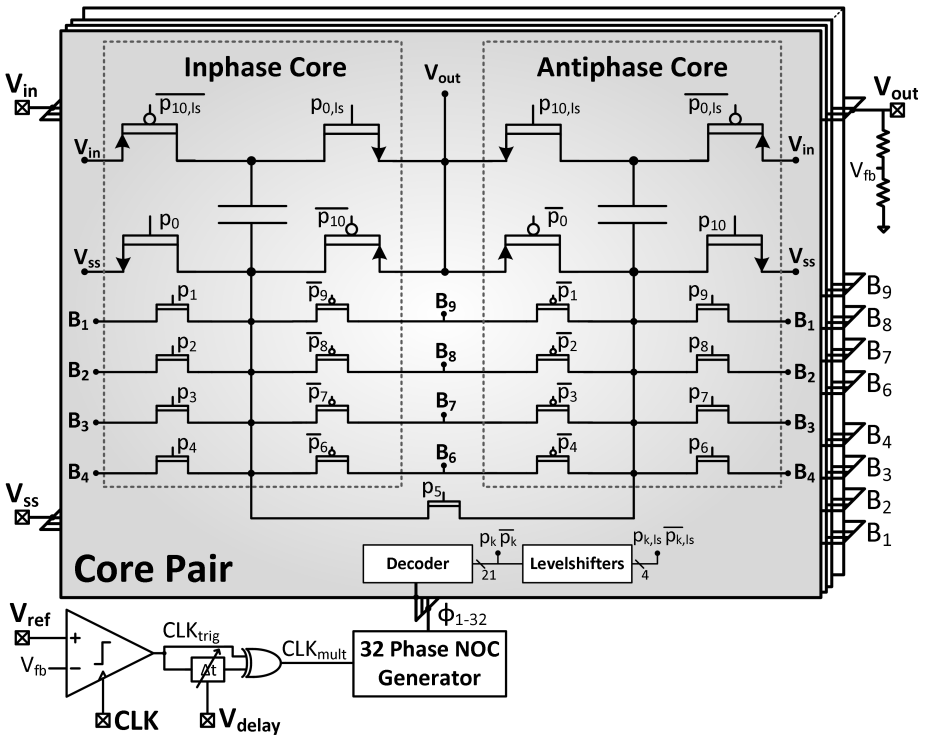

Fig. 9. System overview of the 2:1 converter, showing the controller and transistor-level implementation of the converter cores.

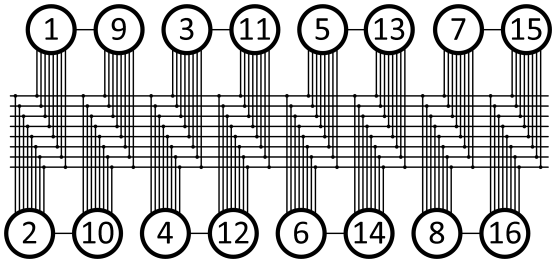

Fig. 10. Core interconnect schema using Charge Redistribution Buses (CRB) and a direct 0.5xV_{out} connection between in- and anti-phase cores.

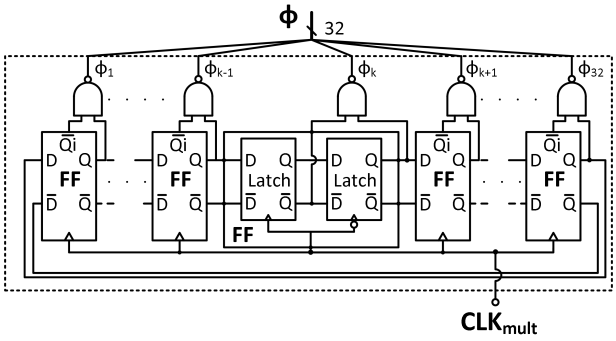

Fig. 11. Implementation of the 32-phase Non-Overlapping-Clock (NOC) generator.

This is done using a XOR-based edge detector with a variable delay block, which passes two pulses at a time to a 32-phase Non-Overlapping-Clock (NOC) generator. The NOC generator, implemented by 32 ring-connected dynamic master-slave Flip-Flops (FF) shown in Fig. 11, is designed such that the width of the pulse determines the non-overlapping time between each of the one-hot coded 32 phases (Fig. 12a). Note that in order to function properly, the FF's need to be initialized such that all but one are in the same state.

All 32-phase signals are subsequently used to locally generate the correct control signals according to the decoding schema shown in Figure 12b or a phase-shifted version thereof. The decoder itself can be efficiently implemented using a total of 9 NAND2 and 9 INV gates for the CRT signals, and 2 Set-Reset (SR) latches for the regular power transistors. Two capacitively coupled levelshifters shift the necessary signals to the high domain (V_{out} to V_{in}) [23]. While efficient, this type of levelshifter does tend to limit the converter's input range. This can be explained as follows: As ($V_{in} - V_{out}$) gets larger relative to V_{out}, the coupling capacitors will achieve less and less of the full swing in the higher domain. Furthermore, thanks to their increasing V_{gst}, the top cross-coupled inverter pair's gain will also increase relative to the gain of the bottom driving buffers. Combined with differences in arrival times of the phase

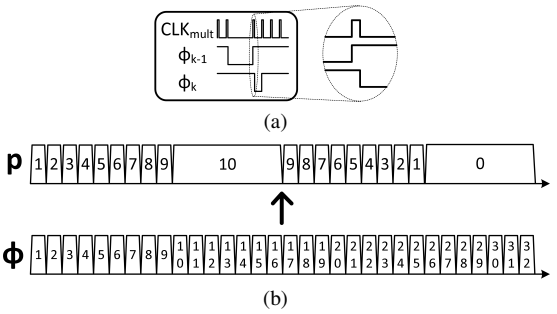

Fig. 12. Details of (a) the non-overlapping phase generation by pulse-width modulation of the clock, and (b) a local decoder schema.

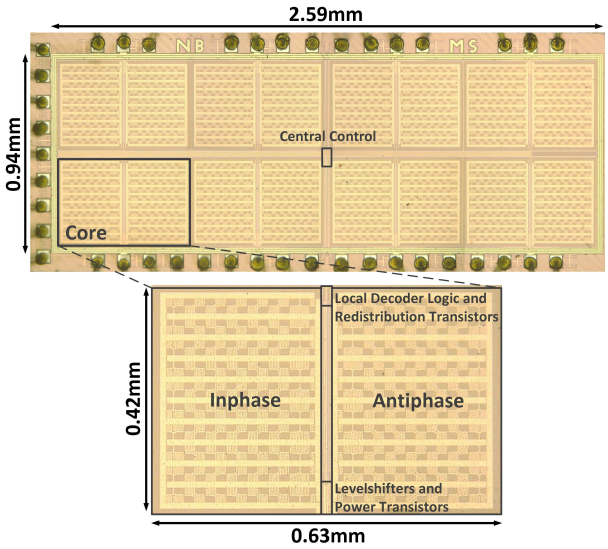

Fig. 13. Annotated micrograph of the fully-integrated 2:1 SC converter using SPCR, measuring $2.4mm^2$ without bond pads.

and anti-phase component of the input of the levelshifter, the signal will eventually no longer be passed on to the higher domain properly.

V. Realization and Measurements

The design is realized in a 40nm baseline CMOS process, using 10nF of MOM capacitance and high-V_T devices to lower the parasitic conductance ratio. Using (17), the theoretical maximum efficiency of the technology was determined to be approximately 89% for a 2:1 conversion. The converter, shown in Fig. 13, measures 0.94x2.59mm^2 without bond pads and has a total active area of $2.2mm^2$. The core pairs are distributed in two rows with the CRB's and control signal interconnections in-between. Their relative placement was optimized for minimal signal interconnect length.

A. Efficiency

Figure 14 shows the converter's measured closed-loop efficiency versus output power for an input voltage

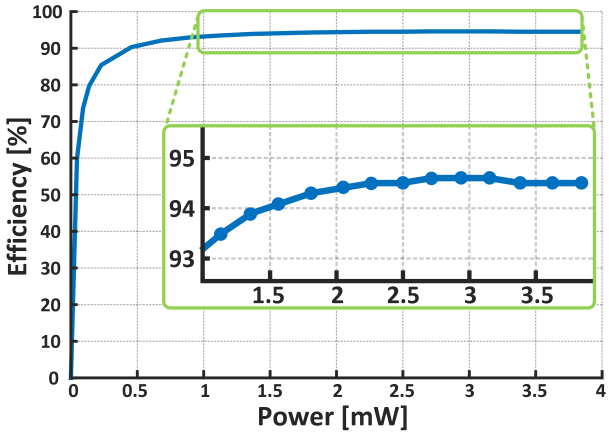

Fig. 14. Measured efficiency versus output power for V_{in}=1.855V and V_{out}=900mV. A peak efficiency of 94.6% is achieved for output powers of 2.7mW to 3.15mW.

and output voltage of 1.855V and 900mV, respectively. The efficiency was measured using Kelvin contacts and includes all system losses. A record efficiency of 94.6% is achieved at an output power of 3.15mW. Due to the input-referred quiescent current of 15μA, the measured efficiency remains high for a wide range of output powers: At 13% of the maximum output power of 3.85mW, the efficiency is still above 90%.

The converter also maintains a high efficiency over its entire usable input voltage range of 215mV, as shown in Fig. 15. The lowest efficiency, measured at the maximal V_{in} of 2.07V, was determined to be 88.6%, which is higher than the previous State-of-the-Art [9]. SPCR does consequently not solely increase the efficiency of the nominal design point, but also boosts the efficiency over the entire voltage range. The VCR-to-VCR_{ideal} ratio, an indication of the converter's conduction losses, reaches a maximum value of 97%, which corresponds to an equivalent drop-out voltage of less than 30mV. This low value can be partly attributed to the symmetrical parasitic coupling of MOM capacitors and the parasitic charging effect discussed in section II-C. Also, note that at the nominal design point, the conduction losses account for slightly more than 50% of the total losses, which conforms to a properly optimized design as shown by (13) and (14).

B. Controller

To validate the hysteretic controller, it is tested under worst-case load-regulation conditions, as shown in Fig. 16. Here, the load current is switched from the nominal load of 4.25mA to zero and back with a transient time of 8ns and with a fixed V_{in} of 1.855V and V_{ref} of 900mV. Without the use of an internal or external output capacitor, C_{DC}, the droop and overshoot are only

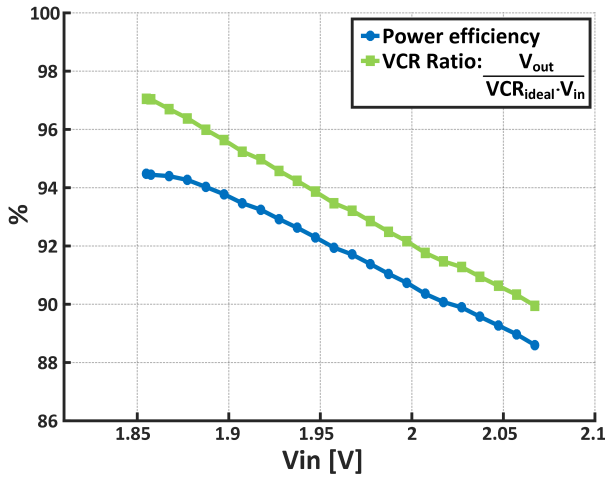

Fig. 15. Measured efficiency and VCR-to-VCR_{ideal} ratio versus V_{in} for a constant load impedance, R_L, and V_{ref} of 212Ω and 900mV respectively.

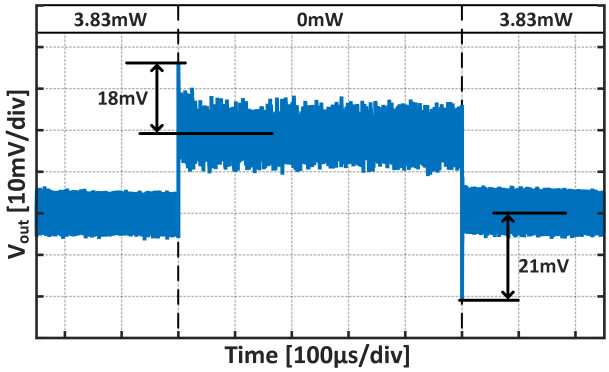

Fig. 16. Full load-step transient response with V_{in}=1.855V and V_{ref}=900mV, with a transient time of 8ns.

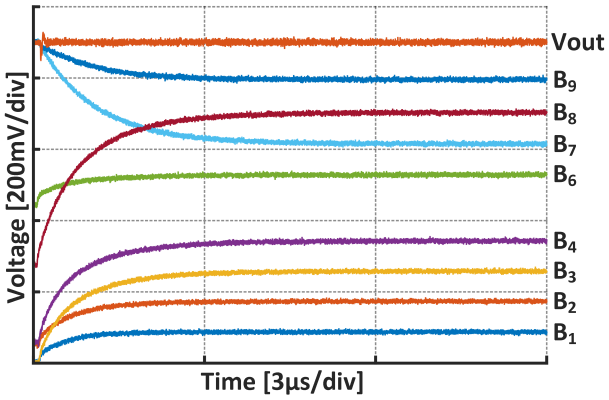

Fig. 17. Start-up of the Charge Redistribution Buses (CRB) with nominal-operation control signals.

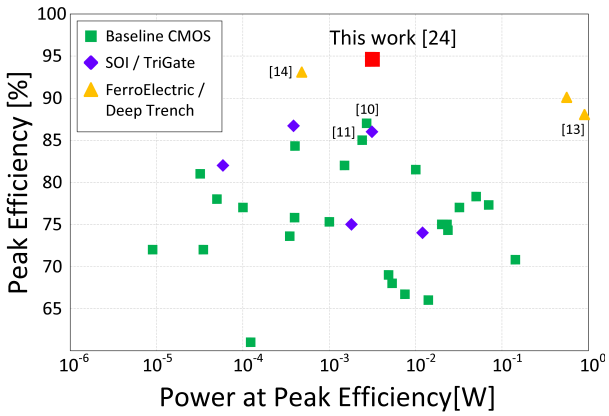

Fig. 18. Visual comparison of this work to the state-of-the-art of fully-integrated closed-loop Switched-Capacitor (SC) converters [9].

21mV and 18mV respectively, showing the fast response capabilities of the lower-bound hysteretic control. The worst-case output voltage ripple, for the nominal input voltage of 1.855V, was found to be 18mV.

C. SPCR Start-up

As mentioned in section II-B, the use of SPCR does not require any kind of initialization because it is inherently stable due to the averaging operation. To support this claim, the start-up of the charge redistribution buses was measured using regular nominal-operation control signals. As can be seen in Fig. 17, the CRB's voltages converge. Furthermore, their steady-state values are evenly spread between ground and V_{out}, which confirms the basic working principle of the CRB's.

D. Comparison

Finally, this work is compared to the state-of-the-art of fully-integrated closed-loop SC converters in Fig. 18 and Table III [24]. Thanks to the presented Scalable Parasitic Charge Redistribution (SPCR) technique, the realized converter achieves a higher efficiency than any other fully-integrated SC regulator, including those using Deep-Trench and Ferro-Electric capacitors which require extra masks. The in this work achieved efficiency of 94.6% is consequently a new record. When comparing for the same 1/2 ratio, thus negating topological differences (K_{BP}, K_c, K_s), the use of SPCR leads to a 68% and 42% reduction in normalized losses compared to bulk CMOS and Ferro-Electric regulators, respectively, which shows the significant advantage SPCR provides.

Furthermore, because SPCR extends naturally on time-interleaving, the presented work realizes a small output voltage ripple without the use of any load capacitance, C_{dc}, and a higher output power and power density compared to other highly-efficient bulk CMOS regulators.

TABLE III
COMPARISON TO STATE-OF-THE-ART.

Item	**This work [24]**	[10]	[11]	[13]	[14]
Technology	**40nm**	90nm	250nm	32nm SOI	130nm
Capacitors	**MOM**	MIM	MIM	Deep-trench	Ferro-Electric
Conversion Ratio's	**1/2**	4/5 2/3	4Bit Recursive	2/3 1/2	1/1 2/3 1/2 1/3
V_{in} $[V]$	**1.855-2.07**	0.7-1.2	2.5	1.8	1.5
V_{out} $[V]$	**0.9**	0.5-0.85	0.1-2.18	0.7-1.1	0.4-1.1
P_L @ η_{peak} $[mW]$	**3.15**	2.7	2.4*	900*	0.48*
Area $[mm^2]$	**2.4**	3	4.65	1.968	0.37
P_D @ η_{peak} $[mW/mm^2]$	**1.3**	0.9	0.52*	460*	1.3*
η_{peak}	**94.6%**	87%	85%	88%*	93%
η_{peak} @ VCR = 1/2	**94.6%**	/	85%*	88%*	91%*
P_N @ VCR = 1/2	**5.7%**	/	17.7%*	13.6%*	9.9%*
V_{ripple} $[mV]$	**18**	60	/	30	/
N	**16**	1	1	64	4
C_{dc} $[nF]$	**0**	3.7*	/	0	/

*estimate based on graphs

VI. CONCLUSION

In this paper the need for highly-efficient fully-integrated voltage regulators and the parasitic substrate coupling as limitation for high efficiency in SC converters were discussed. A novel technique called Scalable Parasitic Charge Redistribution (SPCR) was proposed that reduces these parasitic coupling losses up to any desired level by continuously redistributing parasitic charge in-between phase-shifted converter cores. Because according to previous theoretical models this could lead to efficiencies arbitrarily close to 100%, the effect of transistor leakage was investigated and was found to be another limiting factor in the maximum obtainable efficiency of a SC regulator. Theoretical analysis showed that SPCR significantly increases achievable efficiencies from infinitely low- to very high ($> 10W/mm^2$) power densities and for a wide variety of technological parameters. Thanks to the use of Charge Redistribution Buses (CRB), SPCR only requires little area overhead and is relatively easy to implement. A 1/2 converter has been fabricated in a 40nm bulk CMOS technology and achieved a record fully integrated SC regulator efficiency of 94.6%.

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